

**Notice of References Cited**Application No.  
**09/192,164**Applicant(s)  
**Shawn Smith, et al.**Examiner  
**Jason Greene**Group Art Unit  
**2784**

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**U.S. PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A	5,720,031	2/17/98	Lindsay	714	42
B	5,528,553	6/18/96	Saxena	365	230.01
C	5,475,694	12/12/95	Ivanov et al.	714	732
D	5,469,443	11/21/95	Saxena	714	720
E	4,801,869	1/31/89	Sprogis	714	733
F					
G					
H					
I					
J					
K					
L					
M					

**FOREIGN PATENT DOCUMENTS**

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N						
O						
P						
Q						
R						
S						
T						

**NON-PATENT DOCUMENTS**

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U	Burdick, W.; Duam, W., "High yield multichip modules based on minimal IC pretest", Test Conference, 1994. Proceedings., International, pages 30-40	1994
V	Yue, J.; Liu, S.T.; Fechner, P.; Gardner, G.; Witcraft, W.; Finn, C., "An effective method to screen SOI wafers for mass production", SOI Conference, 1994 Proceedings., 1994 IEEE International, pages 113-114	1994
W	Mullenix, P.; Zaloski, J.; Kasten, A.J., "Limited yield estimation for visual defect sources", Semiconductor Manufacturing, IEEE Transactions on Volume, pages 17-23	10/1997
X	Chen-Pin Kung; Chun-Jieh Huang; Chen-Shang Lin, "Fast fault simulation for BIST applications", Test Symposium, 1995., Proceedings of the Fourth Asian, pages 93-99	1995

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A					
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N						
O						
P						
Q						
R						
S						
T						

**NON-PATENT DOCUMENTS**

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U	Wieler, R.W.; Zhang, Z.; McLeod, R.D., "Using an FPGA based computer as a hardware emulator for built-in self-test structures", Rapid System Prototyping, 1994. Shortening the Path from Specification to Prototype. Proceedings., Fifth International Workshop	1994
V	McLeod, G.R., "Built-in system test and fault location", Proceedings of the 1994 IEEE International test Conference, pages 291-299	1994
W	Hussain, A.; Hayes, J.P., "Design Verification via simulation an automatic test pattern generation", IEEE, pages 174-180	1995
X	Flint, A., "A comparison of test requirements, methods, and results for seven MCM products", test Conference, 1995. Proceedings., International, pages 202-207	1995